REMARKS

Applicants have carefully considered the May 13, 2004 Office Action, and the amendments above together with the comments that follow are presented in a bona fide effort to address all issues raised in that Action and thereby place this case in condition for allowance. Claims 1-18 are pending in this application. In response to the Office Action dated May 13, 2004, claims 1, 12, 14 and 15 have been amended. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the present Amendment should be apparent throughout the originally filed disclosure as, for example, the depicted embodiments and related discussion thereof in the written description of the specification. Entry of the present Amendment is respectfully solicited. It is believed that this response places this case in condition for allowance. Hence, prompt favorable reconsideration of this case is solicited.

The Examiner requested information relating to any co-pending applications that may raise double patenting issues. Applicants are not aware of any co-pending applications at the present time.

The specification was objected to for minor informalities. Applicants have amended the specification to correct the error identified by the Examiner and believe no further amendments are necessary at this time. Accordingly, the Examiner is requested to reconsider and withdraw the objection of the specification.

Claim 14 has been amended to correct the manifest typographical error at line 3 of claim 14. Accordingly, the Examiner is requested to reconsider and withdraw the claim objection.

Claims 1-12 were rejected under 35 U.S.C. § 112 second paragraph. Applicants respectfully traverse. Claims 1, 12 and 15 have been amended to further clarify the claimed subject matter and address the Examiner's concerns.

With respect to claim 1, the boundary scan test circuit is used for testing whether the semiconductor integrated circuit is normally mounted or connected to the on-board interconnection lines after the circuit device is mounted on the board. Therefore, claim 1 has been amended to correct the wording "the mounted state" to "a mounted state of said semiconductor integrated circuit". Moreover, claim 1 is further described at page 19, beginning at line 1, and contrary to the Examiner's assertion that claim 1 is not "clear", one of ordinary skill in art, with the supporting specification in hand, would be able to reasonably ascertain the scope or protection defined by the claim.

As for the power supply in claim 12, the working of "application of a power supply voltage" means that the semiconductor integrated circuit is powered up and the power supply is not required to be connected to the first transistor or the first pad. Claim 12 has been amended to further clarify this limitation. Moreover, claim 12 is further described at page 32, beginning at line 20, and contrary to the Examiner's assertion that claim 12 is not "clear", one of ordinary skill in art, with the supporting specification in hand, would be able to reasonably ascertain the scope or protection defined by the claim.

As for the term "protector" in claim 15, Applicants have canceled this term and have replaced it with the term "inverter" since claim 15 is directed to the decouple transistor as depicted in Fig. 9.

The limitation "thereof" recited in claims 13 and 15 refers to the transfer gate, previously cited in each of claims 13 and 15.

Applicants submit that in view of the preceding remarks and amendments to the claims, that one having ordinary skill in art, with the supporting specification in hand, would be able to reasonably ascertain the scope or protection defined by the claims. Accordingly, the rejection under the second paragraph of 35 U.S.C. § 112 should be withdrawn.

Claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted prior art (AAPA) in view of Ruparel et al., A Vertically Integrated Test Methodology Based on JTAG IEEE 1149.1 Standard Interface; IEEE, (27 Sept. 1991) (hereinafter "Ruparel"). In the statement of the rejection, the Examiner asserted that AAPA substantially discloses the semiconductor integrated circuit of independent claim 1, except for a boundary scan test circuit for testing after the semiconductor integrated circuit is mounted on a printed circuit board. In an attempt to remedy this deficiency the Examiner relied on the secondary reference to Ruparel. The Examiner concluded that it would have been obvious for one of ordinary skill in the art to modify the semiconductor integrated circuit to include the boundary scan test circuit, with the expectation of achieving testing at all levels ranging from the wafer level up to the board and system levels, as suggested by Ruparel. Applicants respectfully traverse.

The Examiner stated in the office action that AAPA indicates the claimed structure and Ruparel discloses the boundary scan test after mounted on a board, and the inventions in the claims are obvious over the combination of these prior art references. Applicants respectfully traverse the rejection and submit that the Examiner has overlooked the problems in the conventional integrated circuit with a bonding optional function as discussed in the present specification. Moreover, it has been held that one having ordinary skill in the art has knowledge of the prior art at the time of the invention. However, it has also been held that one having ordinary skill in the art does not have the benefit of hindsight of Applicants' invention. *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985). As such, the motivation to modify the prior art must come from the prior art and not Applicants' disclosure.

The boundary scan test circuit is connected to external pin terminals in sealing into a BGA package, but is not connected to the external pin terminals in sealing into a QFP package. Therefore, in a QFP package, the terminals of the test circuit is placed in an unstable state to cause

an erroneous operation. The Examiner has simply ignored the problems associated with the prior art circuit device. More importantly, the present invention addresses and solves the problem associated with AAPA.

Moreover, Ruparel does not express any recognition of the problem much less offer any viable solution thereof. Both the recognition and solution to the problem are found only in the Applicant's disclosure, which the Examiner has improperly used in an attempt to establish motivation. However, the motivation must come from the prior art and **not** Applicant's own teaching. Accordingly, the problem addressed and solved by the claimed invention constitutes a potent indicium of nonobviousness which must be given consideration regarding the ultimate legal conclusion of nonobviousness under 35 U.S.C. § 103.

Further, Ruparel discloses a technique based on the premise of a test enabled environment with the boundary scan test circuit supported for an on-board circuit. The Examiner appears to correlate the pad receiving the test mode instruction signal TM with the claimed first pad. However, claim 1 recites the first pad as "having a potential level set according to a type of a package...", and the test mode instruction signal TM has a potential level (logical level) not set in accordance with the type of a package, but set depending on whether the boundary scan test is to be performed. Ergo, even if the applied references are combined as suggested by the Examiner, and an Applicants do not agree that a requisite fact-based motivation has been established, the claimed invention would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). Accordingly, the rejection of claims 1-10 under 35 U.S.C. § 103(a) should be withdrawn.

Dependent claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Ruparel and in further in view of Iketani et al. (U.S. Pat. No. 5,703,510, hereinafter "Iketani"). In the statement of the rejection, the Examiner asserted that AAPA and Ruparel substantially discloses the semiconductor integrated circuit of claim 9, but for an inverter

circuitry means for inverting logic levels of voltages. In an attempt to remedy this deficiency the Examiner relied on Iketani. The Examiner concluded that it would have been obvious for one of ordinary skill in the art to modify the semiconductor integrated circuit to include the inverter circuitry means, with the expectation of preventing erroneous activation of power, as suggested by Iketani. Applicants traverse.

Dependent claim 11 is free from the applied art in view of its dependency from independent claim 1 discussed *supra*. Moreover, Iketani fails to remedy the above described deficiencies of AAPA/Ruparel and, therefore the rejection of claim 11 is not legally viable and should be withdrawn.

Claims 12-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Ruparel and in further in view of Iketani. The Examiner asserted that the limitations of claims 12-18 are similar to the ones of claims 1-11 except for the absence of scanning means. The Examiner merely concluded that claims 12-18 are rejected based on the same rationale as the rejection of claim 11 above. Applicants traverse.

Independent claim 12 describes the arrangement for designating an operation mode of an internal circuit in accordance with a potential on a pad. The phrase "the application of a power supply voltage" in claim 12 describes the power up of the semiconductor integrated circuit, and the first transistor operates in response to the power up to set the pad potential. Iketani discloses a power on reset circuit for generating a power on reset signal upon power up. The claimed subject matter as recited in claim 12 utilizes the power on reset signal generated as in Iketani, to set the pad potential for generating an operation mode instructing signal. Iketani uses the power on reset signal for initializing the internal circuit nodes, and does not use the power on reset signal for generating an operation mode, as claim 12 requires. Thus, even if the applied references are combined as suggested by the Examiner, and an Applicants do not agree that a requisite fact-based motivation

has been established, the claimed invention would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). Accordingly, the rejection of claims 12-18 under 35 U.S.C. § 103(a) should be withdrawn.

It is believed that all pending claims are now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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